Shantilal Shah Engineering College, Bhavnagar

Training & Placement Cell

Feb 16, 2021

Notice: Internship opportunities at OpenFive

OpenFive is a solution-centric silicon company that is uniquely positioned to design processor agnostic SoC architecture, with customizable and differentiated IP for Artificial Intelligence, Edge Computing, HPC, and Networking solutions. OpenFive develops domain-specific SoC architecture based on high-performance, highly efficient, cost-optimized IP to deliver scalable, optimized, differentiated silicon. OpenFive employees work collaboratively to deliver end-to-end expertise in Architecture, Design Implementation, Software, Silicon Validation, and Manufacturing disciplines required to deliver high-quality silicon to semiconductor companies and systems manufacturers. Focused on delivering silicon for customer specifications, no two projects are identical keeping things fresh and offering opportunities to continually develop new skills and meet more people in the semiconductor industry.

Website: https://openfive.com// https://www.sifive.com/

Please find the required details:

Eligibility: BTech/MTech in ECE, EEE, or Electrical and Instrumentation 2021 passing out Only with 70% throughout in academics and zero active backlogs.

Position - Intern

Duration – Only for the 2021 batch for a 6-month internship (conversion based on performance)

Location – Bangalore and Pune

Stipend - INR 25K per month during the internship

PFB the Job Description:

Note:- Please send the student data showing their preferences for the JD.

1:- FPGA Engineer

1) Very good knowledge of at least one hardware description language (Verilog, VHDL)

2) Very good knowledge of System Verilog, UVM is a plus.
3) Very familiar with Altera's or Xilinx's build flow including design entry in Verilog, synthesis, place, and route, timing constraints, and timing closure
4) Hands-on with lab FPGA debug methodologies, such as ChipScope, SignalTap, or others
5) Hands-on experience with lab debug the equipment, such as oscilloscopes and logic analyzers
6) Good understanding of computer architectures
7) Experienced in designing digital circuits
8) Experienced in testing digital circuits in both simulation and hardware
9) Expertise with C/C++

10) Proven experience in FPGA prototyping multi-million gate ASIC design

11) Proven experience in manual/automated design partitioning.
12) Very good understanding of AMBA Protocols
13) Experience with working in Linux environment

14) Experience in bring-up of at-least one of the CPU architecture on FPGA like RISCV/ARM/MIPS CPU is a must.

15) Experience in bring-up at at-least one high-speed interface on FPGA like USB, PCIe, Ethernet, MIPI is a must.

16) Experience in the bring-up of DDR memory interfaces for FPGA is a must.

2:- Embedded Software

1) Candidate should be from ENTC stream.

2) Good understanding of C and assembly.

3) Good understanding on CPU architecture e.g. 8051, ARM, and digital electronics.

4) Good general understanding of operating systems.

5) Any project with a general single-board computer(Arduino RaspberryPi or similar) and Serial slow peripherals covering MCU+ I2C SPI UART etc.

3:- FE:

- Trainees will work on Front End/Analog/Physical design and verification of IPs used in Application-Specific Integrated Circuits (ASICs),
- The work will entail (Chose one based on which field we are choosing the inter for)
    - Logic design/verification using Verilog and System Verilog
    - Various aspects of physical design including STA, LVS/DRC, Florrplanning P&R
    - Schematic Design, Analog, and Analog Mixed Signal simulations Custom Layout design
- Trainees must demonstrate the ability to learn quickly, rapidly master complex tasks, and quickly build a high level of competency in Unix and scripting with languages such as Tcl, Perl, or Python.
- To qualify for the traineeship, candidates must demonstrate a sound understanding
    - Digital design and verification concepts
    - Analog design concepts
    - of CMOS technology, CMOS logic circuits, and sequential circuit timing.
- A good grasp of electronic engineering fundamentals is essential.
- Candidates must also be able to code in any programming language.

For further queries and information, you can reach out to:

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